Title: **Sub-threshold Computational Circuits for High-order Data-driven Analysis of Physiological Signals**

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Thanks to emerging sensing and acquisition technologies, wearable and implantable systems are able to access physiologically-indicative signals (e.g., ECG, EEG, ECoG, LFPs, etc.) at low power levels [1], making possible devices of potentially high scientific and clinical value. The signals, however, represent the superposition of many simultaneous physiological processes. Detecting targeted states therefore requires high-order analysis. Sub-threshold computational devices have been demonstrated for basic but low-energy signal processing [2,3]. Higher-order signal models incur substantially higher computational power, challenging the viability of advanced analysis in wearable and implantable devices [4].

Data-driven methods, based on supervised machine learning, provide a powerful framework for creating and applying high-order models for physiological signal analysis [5]. This work explores methods to dramatically reduce the energy of the kernel computations involved by exploiting the parallelism that they potentially offer. The throughput requirements for real-time signal analysis can thus be met at substantially reduced energy levels through low-voltage operation.

The framework used is the support-vector machine (SVM), which enables efficient construction of high-order models by first training on signal features. Detection of targeted states then involves computing signal features and classifying these in real time. Case studies (of neurological and cardiac signal-analysis applications) show that the model complexity required in biomedical detectors will cause the classifier power to dominate by orders of magnitude over feature computation or instrumentation. A classifier is demonstrated that exploits parallelism to permit real-time detection at a sub-threshold minimum-energy point of 0.4V for the supply voltage. In simulation, the classifier operates at 1MHz (500kHz W.C.), and performs the equivalent of 7M MACs/sec, consuming less than 3uJ per classification (the applications require 1-3 classifications/sec). Hardware configurability permits precision scaling of the inputs from 8-12 bits and selectability between classifier transformation functions. The classifier is designed and optimized for model programmability through low-energy readout memories.

References:

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