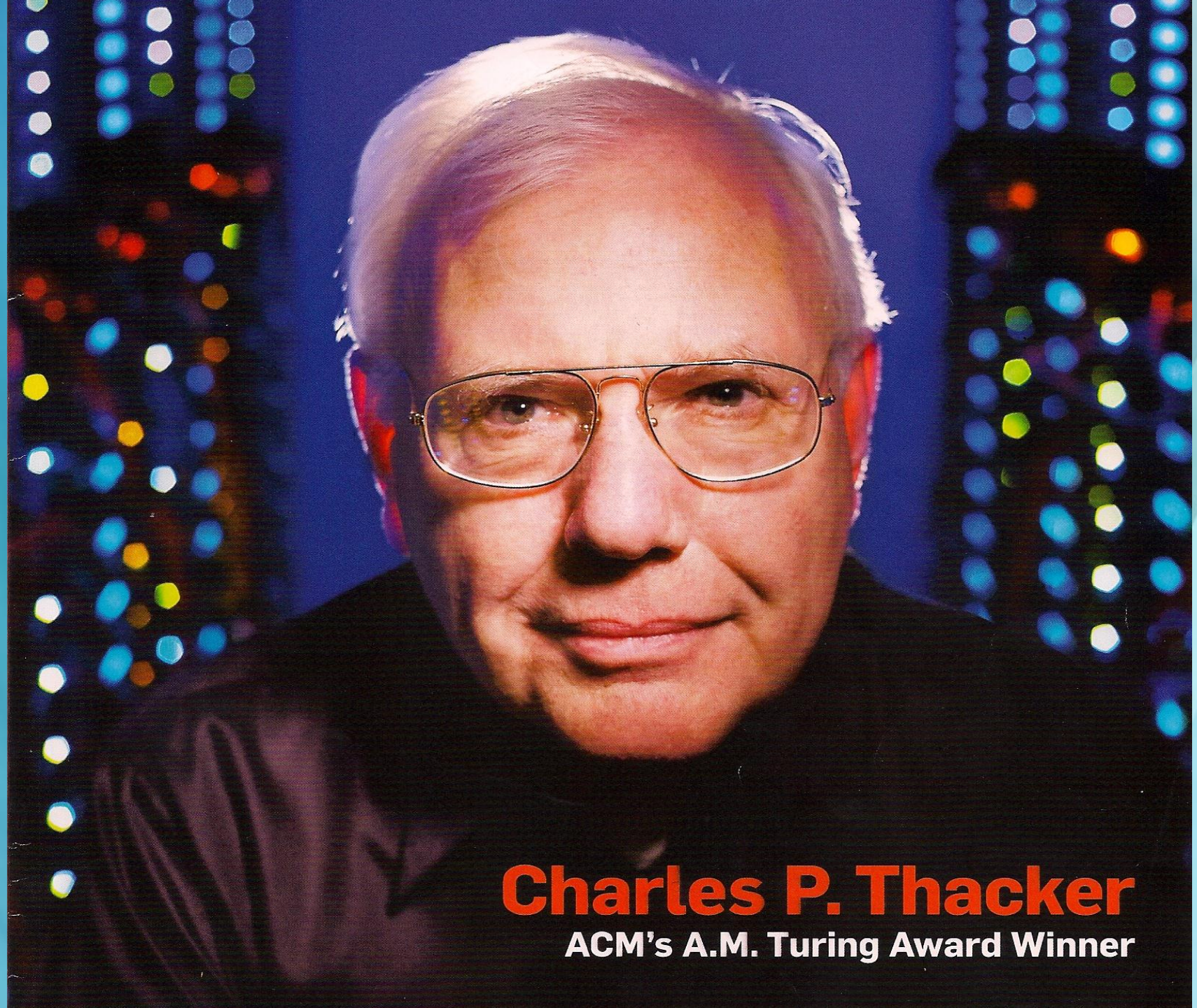
Microsoft® Research

Faculty Summit 2010

Announcements

- The Dinner Cruise will depart from the Kirkland Dock at 6:30PM.
- Buses from here are going straight to the boat without stopping at the hotel.
- Remember to take your coats and bags with you off of the bus and onto the boat; There is luggage check on the boat.
- At the end of the cruise, buses will return to the Conference Center and the hotels.


Charles P. Thacker
ACM's A.M. Turing Award Winner

Microsoft® Research

Faculty Summit 2010

Chuck Thacker
Technical Fellow

RARE: Rethinking Architecture Research and Education

Chuck Thacker (cthacker@microsoft.com)
Microsoft Research Silicon Valley
12 July 2010

Influential D. Patterson columns:

Seven Reason to Shave Your Head and Three Reasons Not to: The bald truth. Commun. ACM. 49, (4): 31-32 (April, 2006)

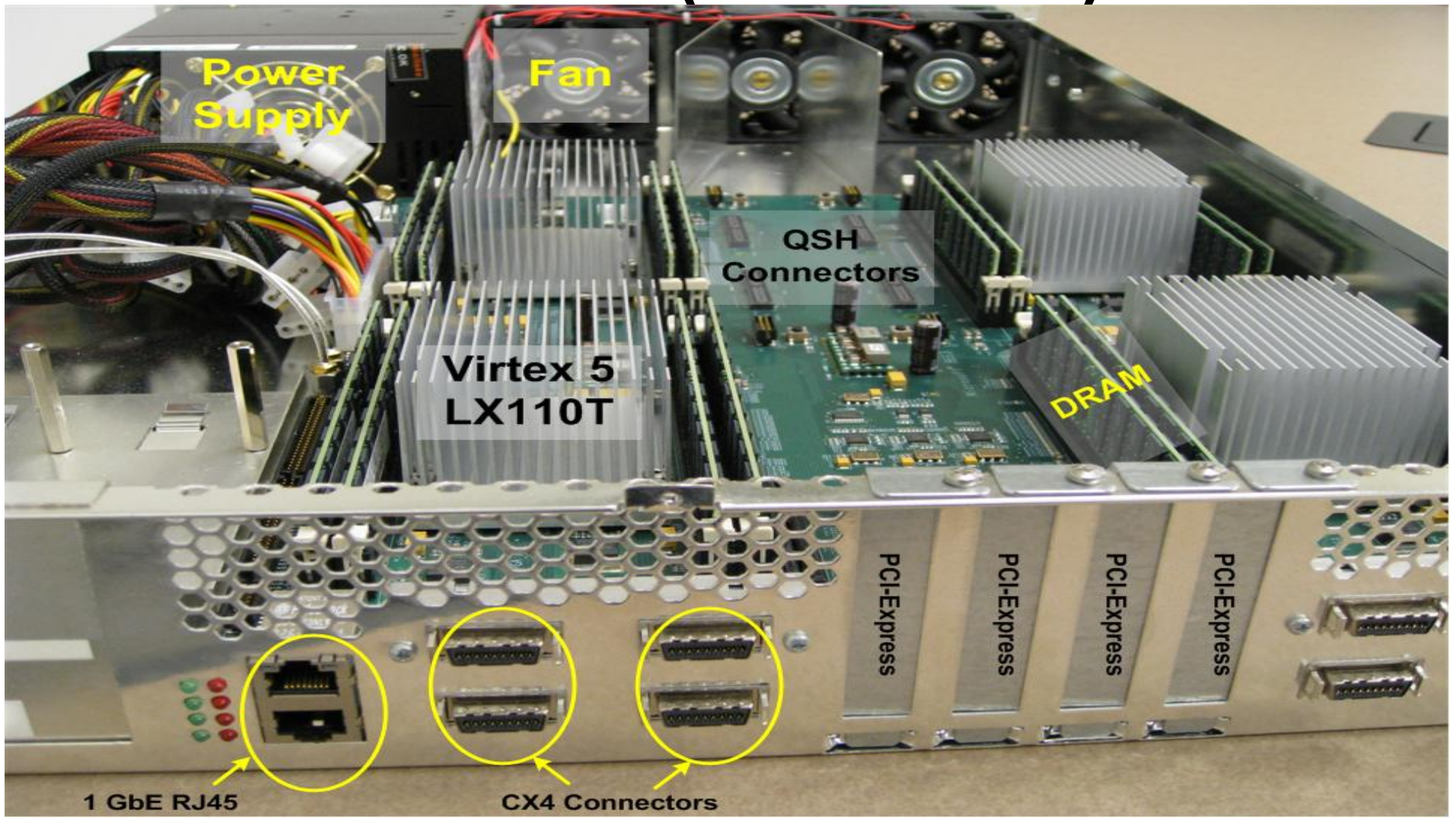
Computer Science Education in the 21st Century. Commun. ACM 49, (3): 27-30 (March, 2006)

Alas, sometimes, Dave is wrong…

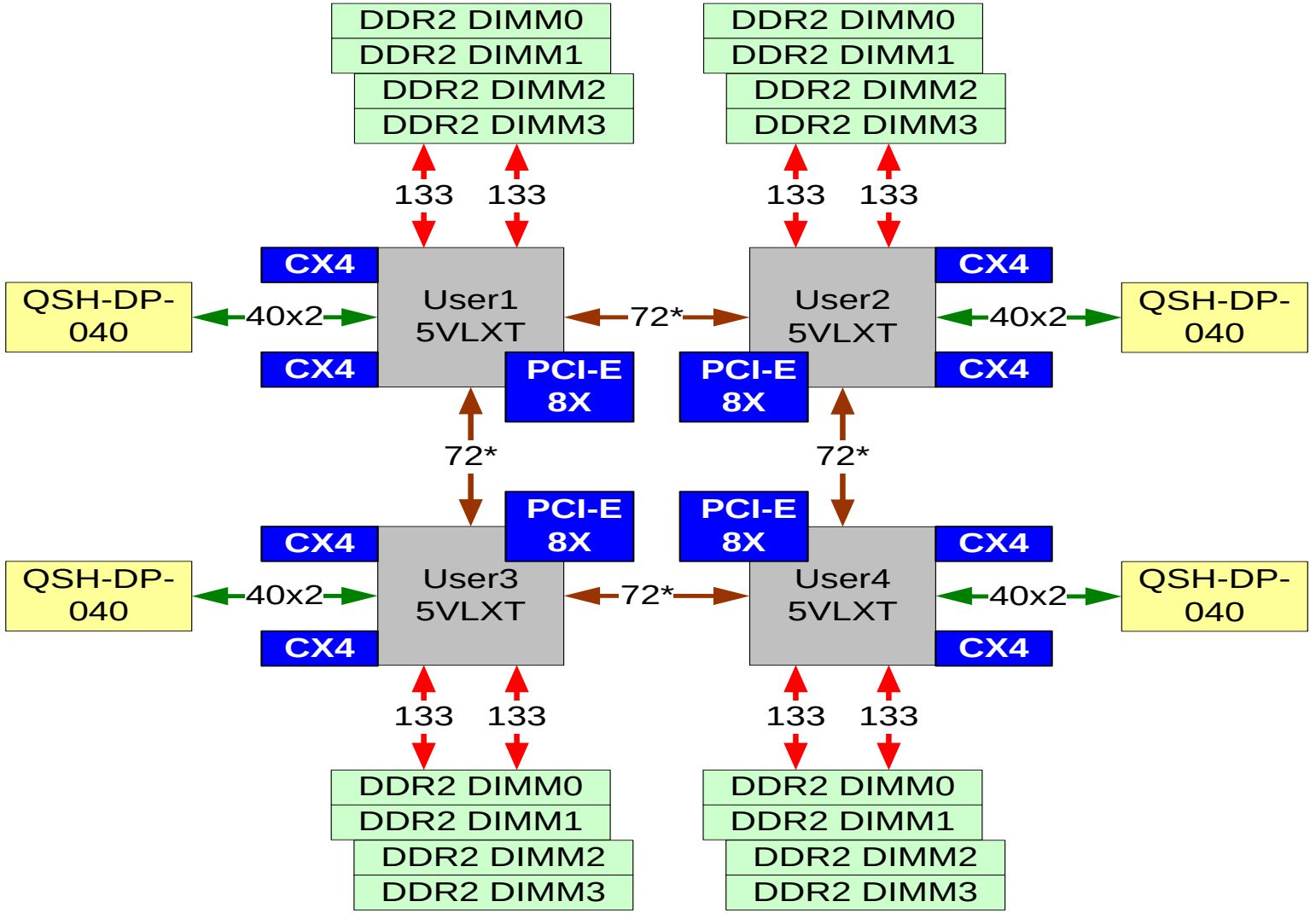
Points in Dave's second CACM column:

- Use tools and libraries
  - "For many CS courses, a dramatic change would simply be if students first wrote a clear specification and then built software using modern tools and software components".
- Embrace Parallelism.
- Join the OS movement.
- Build your own supercomputer.
  - Described *RAMP*, which led to my latest projects.

BEE3 (‘06 – ’09)


Power Supply
Fan
QSH Connectors
Virtex 5 LX110T
DRAM
PCI-Express
PCI-Express
PCI-Express
PCI-Express
1 GbE RJ45
CX4 Connectors

BEE3 Subsystems



BEE3 Program

- MSR, UCB did the detailed specifications
- MSR engaged Celestica for the implementation.
  - Better than burning out grad students
  - Pros can do the job better and faster
  - Resulting board worked the first time (unprecedented for me)
- MS licensed the design to a 3rd party company (BEECube) to build, sell, and support systems.
  - ~75 shipped to date
  - MSR supplied some basic IP (DRAM controller)
- Means that both academics and industrial customers can buy them.
  - Not the case if NSF/DARPA funded

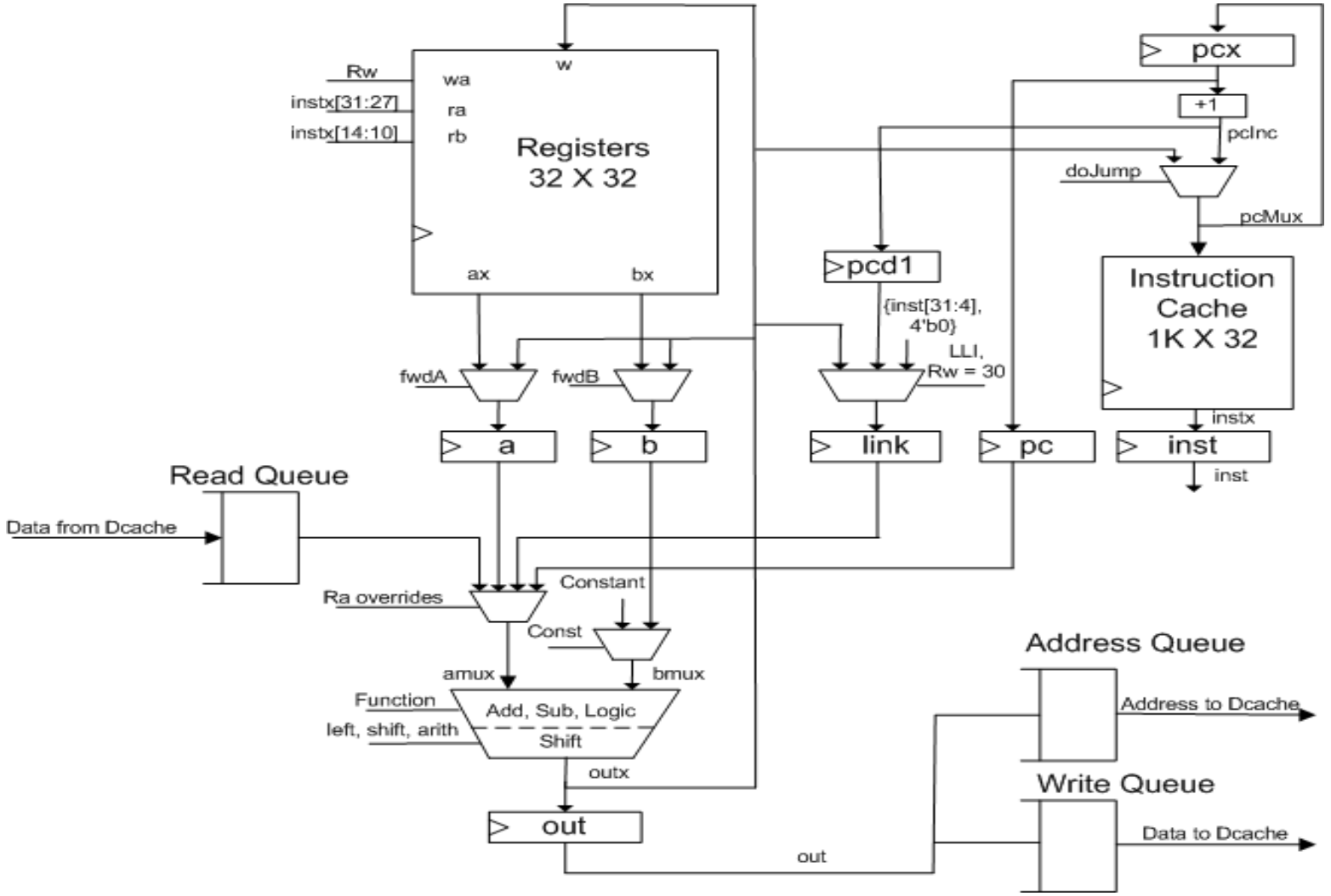
Beehive ('09 – present)

- An FPGA-based many-core system
  - 13 RISC cores (100 MHz)
  - 2 GB DDR2 DRAM controller
  - Display controller
  - 1 Gb Ethernet controller
  - ~6K lines of Verilog
  - Students can understand *and modify* it, using only the basic Xilinx tools (ISE, ChipScope). No high-powered CAD needed.
- A software tool chain
  - C compiler, assembler, linker
- A small but growing set of libraries for frequently needed things
- Licensed for academic research use

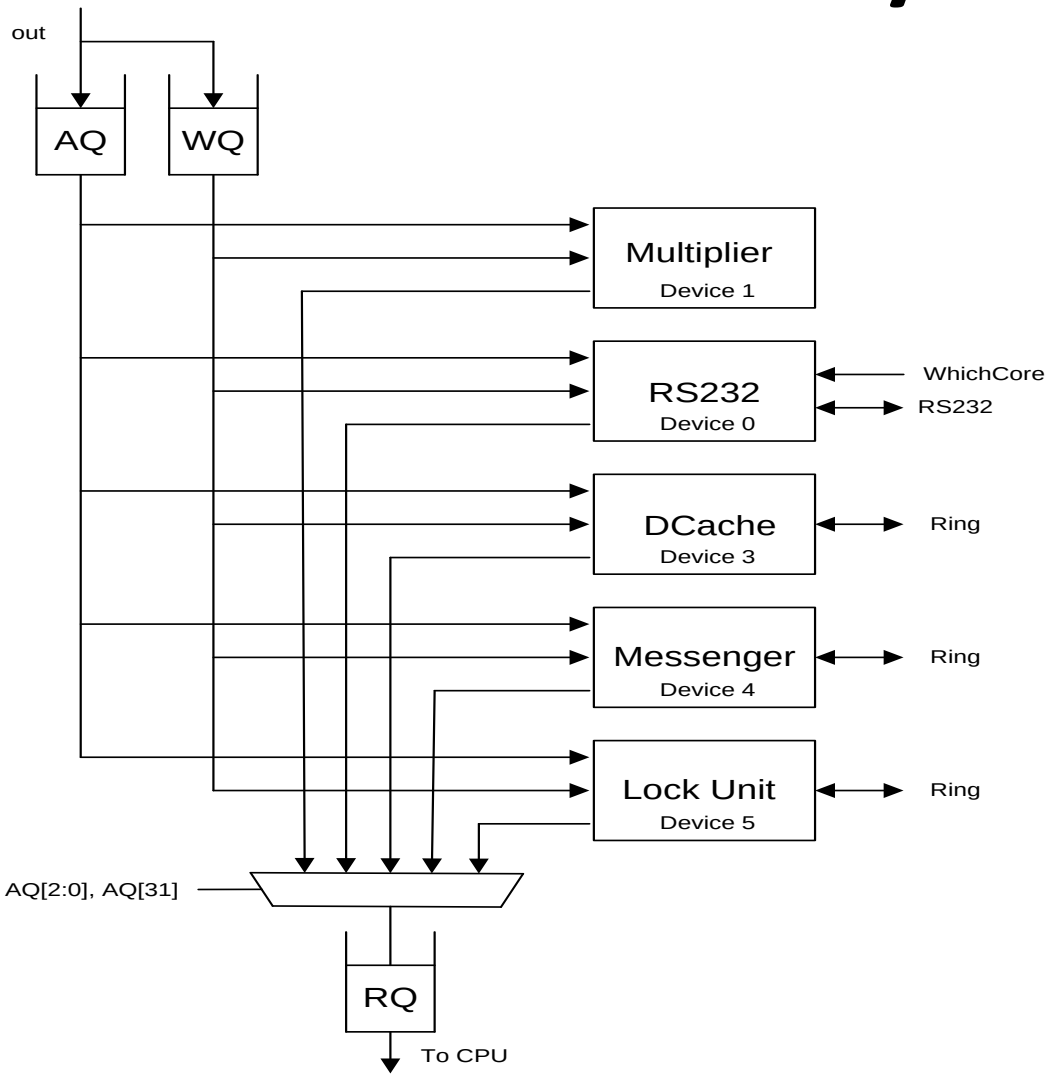
Beehive on Xilinx XUPV5

Academic price: $750

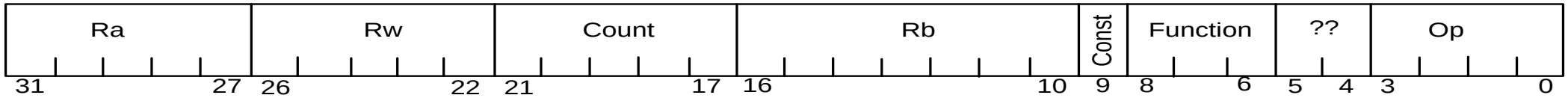
Beehive Core CPU



Core local IO subsystem



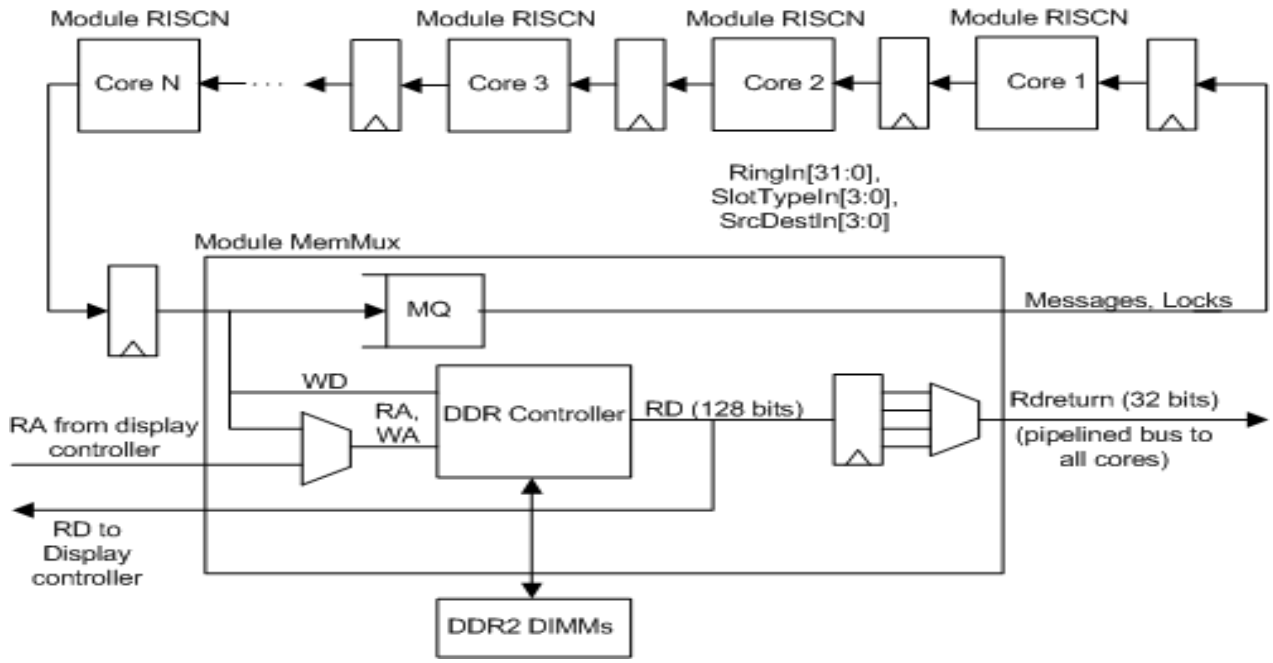
Beehive instructions



- 32-bit instructions, 32-bit registers
- Rw = Ra Function Rb Op Count
  - Function: add, sub, logic
  - Op: Shifts
- Variants for Jumps, Memory accesses
- Support for constants

Beehive Ring Interconnect

- All wires are local
- Passes through:
  - Each core
  - Display controller
  - Ethernet controller
  - DRAM controller
- "Train" contains token + contents
- Each node can modify/append to the train



Architectural Curiosities

- No coherent memory
- No byte addressing
  - We fudge this
- No protection
  - We may add this
- No VM
- No kernel mode

Beehive uses: Education

- Architecture lab courses
  - Boards are inexpensive, so every student can have one.
  - Verilog is simple enough for students to make changes, try new things.
    - Like Stanford's NetFPGA
  - Tool chain and libraries are familiar
    - GCC, make,…
  - Initial results are promising

Beehives at MIT

Two-week IAP course in January, full-semester course in Fall ’10.

Xilinx donated 20 boards.

Students modified the Verilog and successfully tested their changes.

http://projects.csail.mit.edu/beehive

Beehive uses: Research

- Forget shared memory. Use message passing
- Transactional memory.
  - Allows apples-to-apples comparison with Monitors/CVs
  - Gets coherence where you need it.
- Do we really need…
  - Coherent shared memory?
  - Interrupts?
  - VM?
  - An OS?

Beehive Non-goals

- Emulate an existing ISA
  - Modern ISAs are *not* simple
  - Can't do direct comparisons, only A/B experiments.
- Run Linux or other extant OSes
  - Small test programs, benchmarks
  - Barrelfish is the exception
- Have high performance
  - Can't have this with FPGAs anyway.
  - Only needs to be fast enough to run programs much faster than a simulator.

Next steps

- Port (back) to BEE3
- Use in our own research
- TM (MSR SVL)
- Barrelfish (MSR Cambridge, ETH)
- Make it more widely available for academic use (email me)

Q&A

Microsoft® Research

Faculty Summit 2010

Announcements

- The Dinner Cruise will depart from the Kirkland Dock at 6:30PM.
- Buses from here are going straight to the boat without stopping at the hotel.
- Remember to take your coats and bags with you off the bus and onto the boat; There is no luggage check on the boat.
- At the end of the cruise, buses will return to the Conference Center and the hotels.

Microsoft® Research

Faculty Summit 2010